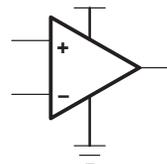


TLV271, TLV272, TLV274 FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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- Rail-To-Rail Output
- Wide Bandwidth . . . 3 MHz
- High Slew Rate . . . 2.4 V/ μ s
- Supply Voltage Range . . . 2.7 V to 16 V
- Supply Current . . . 550 μ A/Channel
- Input Noise Voltage . . . 39 nV/ $\sqrt{\text{Hz}}$
- Input Bias Current . . . 1 pA
- Specified Temperature Range
 - 0°C to 70°C . . . Commercial Grade
 - 40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging
 - 5 Pin SOT-23 (TLV271)
 - 8 Pin MSOP (TLV272)
- Ideal Upgrade for TLC27x Family

Operational Amplifier



description

The TLV27x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range while adding the rail-to-rail output swing feature. This makes it an ideal alternative to the TLC27x family for applications where rail-to-rail output swings are essential. The TLV27x also provides 3-MHz bandwidth from only 550 μ A.

Like the TLC27x, the TLV27x is fully specified for 5-V and \pm 5-V supplies. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from a variety of rechargeable cells (\pm 8 V supplies down to \pm 1.35 V).

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an attractive alternative for the TLC27x in battery-powered applications.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micropower microcontrollers available today including TI's MSP430.

SELECTION OF SIGNAL AMPLIFIER PRODUCTS†

| DEVICE | V _{DD} (V) | V _{IO} (μ V) | I _q /Ch (μ A) | I _{IB} (pA) | GBW (MHz) | SR (V/ μ s) | SHUTDOWN | RAIL-TO-RAIL | SINGLES/DUALS/QUADS |
|---------|---------------------|----------------------------|-------------------------------|----------------------|-----------|-----------------|----------|--------------|---------------------|
| TLV27x | 2.7–16 | 500 | 550 | 1 | 3 | 2.4 | — | O | S/D/Q |
| TLC27x | 3–16 | 1100 | 675 | 1 | 1.7 | 3.6 | — | — | S/D/Q |
| TLV237x | 2.7–16 | 500 | 550 | 1 | 3 | 2.4 | Yes | I/O | S/D/Q |
| TLC227x | 4–16 | 300 | 1100 | 1 | 2.2 | 3.6 | — | O | D/Q |
| TLV246x | 2.7–6 | 150 | 550 | 1300 | 6.4 | 1.6 | Yes | I/O | S/D/Q |
| TLV247x | 2.7–6 | 250 | 600 | 2 | 2.8 | 1.5 | Yes | I/O | S/D/Q |
| TLV244x | 2.7–10 | 300 | 725 | 1 | 1.8 | 1.4 | — | O | D/Q |

† Typical values measured at 5 V, 25°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TLV271, TLV272, TLV274

FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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FAMILY PACKAGE TABLE

| DEVICE | NUMBER OF CHANNELS | PACKAGE TYPES | | | | | SHUTDOWN | UNIVERSAL EVM BOARD |
|--------|--------------------|---------------|------|--------|-------|------|----------|---|
| | | PDIP | SOIC | SOT-23 | TSSOP | MSOP | | |
| TLV271 | 1 | 8 | 8 | 5 | — | — | — | Refer to the EVM Selection Guide (Lit# SLOU060) |
| TLV272 | 2 | 8 | 8 | — | — | 8 | — | |
| TLV274 | 4 | 14 | 14 | — | 14 | — | — | |

TLV271 AVAILABLE OPTIONS

| T _A | V _{IO} MAX AT 25°C | PACKAGED DEVICES | | | |
|----------------|-----------------------------|--------------------------------|--------------------|--------|-----------------|
| | | SMALL OUTLINE (D) [†] | SOT-23 | | PLASTIC DIP (P) |
| | | | (DBV) [‡] | SYMBOL | |
| 0°C to 70°C | 5 mV | TLV271CD | TLV271CDBV | VBHC | — |
| –40°C to 125°C | | TLV271ID | TLV271IDBV | VBHI | TLV271IP |

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV271IDR).

[‡] This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an R suffix (e.g., TLV270IDBVR). For smaller quantities (250 pieces per mini-reel), add a T suffix to the part number (e.g., TLV270IDBVT).

TLV272 AVAILABLE OPTIONS

| T _A | V _{IO} MAX AT 25°C | PACKAGED DEVICES | | | |
|----------------|-----------------------------|--------------------------------|--------------------|--------|-----------------|
| | | SMALL OUTLINE (D) [§] | MSOP | | PLASTIC DIP (P) |
| | | | (DGK) [§] | SYMBOL | |
| 0°C to 70°C | 5 mV | TLV272CD | TLV272CDGK | AVF | — |
| –40°C to 125°C | | TLV272ID | TLV272IDGK | AVG | TLV272IP |

[§] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV272IDR).

TLV274 AVAILABLE OPTIONS

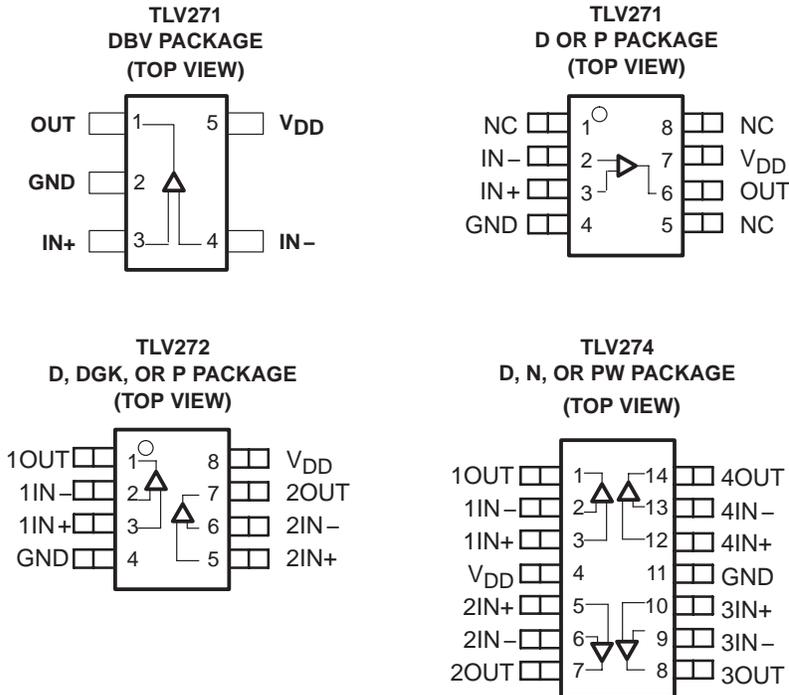
| T _A | V _{IO} MAX AT 25°C | PACKAGED DEVICES | | |
|----------------|-----------------------------|--------------------------------|-----------------|-------------------------|
| | | SMALL OUTLINE (D) [¶] | PLASTIC DIP (N) | TSSOP (PW) [¶] |
| 0°C to 70°C | 5 mV | TLV274CD | — | TLV274CPW |
| –40°C to 125°C | | TLV274ID | TLV274IN | TLV274IPW |

[¶] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV274IDR).

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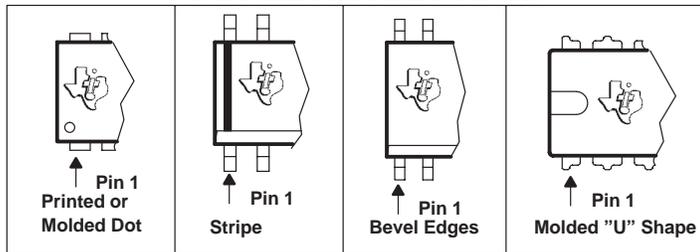
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TLV27x PACKAGE PINOUTS(1)



NC – No internal connection
(1) SOT-23 may or may not be indicated

TYPICAL PIN 1 INDICATORS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|------------------------------|
| Supply voltage, V_{DD} (see Note 1) | 16.5 V |
| Differential input voltage, V_{ID} | $\pm V_{DD}$ |
| Input voltage range, V_I (see Note 1) | -0.2 V to $V_{DD} + 0.2$ V |
| Input current range, I_I | ± 10 mA |
| Output current range, I_O | ± 100 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : C suffix | 0°C to 70°C |
| I suffix | -40°C to 125°C |
| Maximum junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | θ_{JC} (°C/W) | θ_{JA} (°C/W) | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 25^\circ\text{C}$ POWER RATING |
|------------|-------------------------|-------------------------|---|--|
| D (8) | 38.3 | 176 | 710 mW | 396 mW |
| D (14) | 26.9 | 122.3 | 1022 mW | 531 mW |
| D (16) | 25.7 | 114.7 | 1090 mW | 567 mW |
| DBV (5) | 55 | 324.1 | 385 mW | 201 mW |
| DBV (6) | 55 | 294.3 | 425 mW | 221 mW |
| DGK (8) | 54.23 | 259.96 | 481 mW | 250 mW |
| DGS (10) | 54.1 | 257.71 | 485 mW | 252 mW |
| N (14, 16) | 32 | 78 | 1600 mW | 833 mW |
| P (8) | 41 | 104 | 1200 mW | 625 mW |
| PW (14) | 29.3 | 173.6 | 720 mW | 374 mW |
| PW (16) | 28.7 | 161.4 | 774 mW | 403 mW |

recommended operating conditions

| | | MIN | MAX | UNIT |
|--|---------------|------------|-----------------|------|
| Supply voltage, V_{DD} | Single supply | 2.7 | 16 | V |
| | Split supply | ± 1.35 | ± 8 | |
| Common-mode input voltage range, V_{ICR} | | 0 | $V_{DD} - 1.35$ | V |
| Operating free-air temperature, T_A | C-suffix | 0 | 70 | °C |
| | I-suffix | -40 | 125 | |

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electrical characteristics at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted)

dc performance

| PARAMETER | | TEST CONDITIONS | | T_A † | MIN | TYP | MAX | UNIT |
|----------------|---|---|--|------------|-----|-----|-----|------------------------------|
| V_{IO} | Input offset voltage | $V_{IC} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$, | $V_O = V_{DD}/2$, $R_S = 50\ \Omega$ | 25°C | 0.5 | | 5 | mV |
| | | | | Full range | | | 7 | |
| α_{VIO} | Offset voltage drift | | | 25°C | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| $CMRR$ | Common-mode rejection ratio | $V_{IC} = 0\text{ to }V_{DD}-1.35\text{V}$, $R_S = 50\ \Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 58 | | 70 | dB |
| | | | | Full range | | 55 | | |
| | | $V_{IC} = 0\text{ to }V_{DD}-1.35\text{V}$, $R_S = 50\ \Omega$, | $V_{DD} = 5\text{ V}$ | 25°C | 65 | | 80 | |
| | | | | Full range | | 62 | | |
| | | $V_{IC} = -5\text{ to }V_{DD}-1.35\text{V}$, $R_S = 50\ \Omega$, | $V_{DD} = \pm 5\text{ V}$ | 25°C | 69 | | 85 | |
| | | | | Full range | | 66 | | |
| A_{VD} | Large-signal differential voltage amplification | $V_{O(PP)} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 97 | | 106 | dB |
| | | | | Full range | | 76 | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 100 | | 110 | |
| | | | | Full range | | 86 | | |
| | | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 100 | | 115 | |
| | | | | Full range | | 90 | | |

† Full range is 0°C to 70°C for C suffix and full range is -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

input characteristics

| PARAMETER | | TEST CONDITIONS | | T_A | MIN | TYP | MAX | UNIT |
|------------|-------------------------------|--|---------------------|-------|-----|------|------|------------|
| I_{IO} | Input offset current | $V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$ | | 25°C | | 1 | 60 | pA |
| | | | | 70°C | | | 100 | |
| | | | | 125°C | | | 1000 | |
| I_{IB} | Input bias current | | | 25°C | | 1 | 60 | pA |
| | | | | 70°C | | | 100 | |
| | | | | 125°C | | | 1000 | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | | 1000 | | G Ω |
| C_{IC} | Common-mode input capacitance | | $f = 21\text{ kHz}$ | 25°C | | 8 | | pF |

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electrical characteristics at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted)

output characteristics

| PARAMETER | TEST CONDITIONS | T_A † | MIN | TYP | MAX | UNIT |
|------------------------------------|---|---------------------------|------------|-------|-------|------|
| V_{OH} High-level output voltage | $V_{IC} = V_{DD}/2$, $I_{OH} = -1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.55 | 2.58 | V |
| | | | Full range | 2.48 | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 4.9 | 4.93 | |
| | | | Full range | 4.85 | | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 4.92 | 4.96 | |
| | | | Full range | 4.9 | | |
| | $V_{IC} = V_{DD}/2$, $I_{OH} = -5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 1.9 | 2.1 | |
| | | | Full range | 1.5 | | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 4.6 | 4.68 | |
| | | | Full range | 4.5 | | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 4.7 | 4.84 | |
| | | | Full range | 4.65 | | |
| V_{OL} Low-level output voltage | $V_{IC} = V_{DD}/2$, $I_{OL} = 1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.1 | 0.15 | V |
| | | | Full range | | 0.22 | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 0.05 | 0.1 | |
| | | | Full range | | 0.15 | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | -4.95 | -4.92 | |
| | | | Full range | | -4.9 | |
| | $V_{IC} = V_{DD}/2$, $I_{OL} = 5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 0.5 | 0.7 | |
| | | | Full range | | 1.1 | |
| | | $V_{DD} = 5\text{ V}$ | 25°C | 0.28 | 0.4 | |
| | | | Full range | | 0.5 | |
| | | $V_{DD} = \pm 5\text{ V}$ | 25°C | -4.84 | -4.7 | |
| | | | Full range | | -4.65 | |
| I_O Output current | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 2.7\text{ V}$ | Positive rail | 25°C | 4 | mA | |
| | | Negative rail | 25°C | 5 | | |
| | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 5\text{ V}$ | Positive rail | 25°C | 7 | | |
| | | Negative rail | 25°C | 8 | | |
| | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 10\text{ V}$ | Positive rail | 25°C | 13 | | |
| | | Negative rail | 25°C | 12 | | |

† Full range is 0°C to 70°C for C suffix and full range is -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.

‡ Depending on package dissipation rating

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electrical characteristics at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V , and $\pm 5\text{ V}$ (unless otherwise noted) (continued)

power supply

| PARAMETER | | TEST CONDITIONS | T_A † | MIN | TYP | MAX | UNIT |
|------------|--|--|-------------------------|------------|-----|-----|---------------|
| I_{DD} | Supply current (per channel) | $V_O = V_{DD}/2$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 470 | 560 | μA |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 550 | 660 | |
| | | | $V_{DD} = 10\text{ V}$ | 25°C | 625 | 800 | |
| Full range | | | | 1000 | | | |
| PSRR | Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 2.7\text{ V to } 16\text{ V}$, No load | $V_{IC} = V_{DD}/2$ | 25°C | 70 | 80 | dB |
| | | | | Full range | 65 | | |

† Full range is 0°C to 70°C for C suffix and full range is –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

dynamic performance

| PARAMETER | | TEST CONDITIONS | T_A † | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|--|---------------------------------------|------------|------|-----|------------------------|
| UGBW | Unity gain bandwidth | $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$ | $V_{DD} = 2.7\text{ V}$ | 25°C | 2.4 | | MHz |
| | | | $V_{DD} = 5\text{ V to } 10\text{ V}$ | 25°C | 3 | | |
| SR | Slew rate at unity gain | $V_{O(PP)} = V_{DD}/2$, $C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, | $V_{DD} = 2.7\text{ V}$ | 25°C | 1.35 | 2.1 | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 1 | | |
| | | | $V_{DD} = 5\text{ V}$ | 25°C | 1.45 | 2.4 | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 1.2 | | |
| | | | $V_{DD} = \pm 5\text{ V}$ | 25°C | 1.8 | 2.6 | $\text{V}/\mu\text{s}$ |
| | | | | Full range | 1.3 | | |
| ϕ_m | Phase margin | $R_L = 2\text{ k}\Omega$ | $C_L = 10\text{ pF}$ | 25°C | 65 | | ° |
| | Gain margin | $R_L = 2\text{ k}\Omega$ | $C_L = 10\text{ pF}$ | 25°C | 18 | | dB |
| t_s | Settling time | $V_{DD} = 2.7\text{ V}$, $V(\text{STEP})_{PP} = 1\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 2\text{ k}\Omega$ | 0.1% | 25°C | 2.9 | | μs |
| | | $V_{DD} = 5\text{ V, } \pm 5\text{ V}$, $V(\text{STEP})_{PP} = 1\text{ V}$, $A_V = -1$, $C_L = 47\text{ pF}$, $R_L = 2\text{ k}\Omega$ | 0.1% | | 2 | | |

† Full range is 0°C to 70°C for C suffix and full range is –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

noise/distortion performance

| PARAMETER | | TEST CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------|---|-------------|------|-------|------------------------------|------|
| THD + N | Total harmonic distortion plus noise | $V_{DD} = 2.7\text{ V}$, $V_{O(PP)} = V_{DD}/2\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ kHz}$ | $A_V = 1$ | 25°C | 0.02% | | |
| | | | $A_V = 10$ | | 0.05% | | |
| | | | $A_V = 100$ | | 0.18% | | |
| | | $V_{DD} = 5\text{ V, } \pm 5\text{ V}$, $V_{O(PP)} = V_{DD}/2\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 10\text{ K}$ | $A_V = 1$ | 25°C | 0.02% | | |
| | | | $A_V = 10$ | | 0.09% | | |
| | | | $A_V = 100$ | | 0.50% | | |
| V_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ | 25°C | 39 | | $\text{nV}/\sqrt{\text{Hz}}$ | |
| | | $f = 10\text{ kHz}$ | | 35 | | | |
| I_n | Equivalent input noise current | $f = 1\text{ kHz}$ | 25°C | 0.6 | | $\text{fA}/\sqrt{\text{Hz}}$ | |

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TYPICAL CHARACTERISTICS

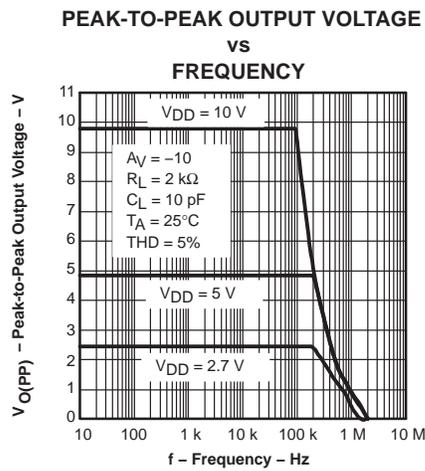
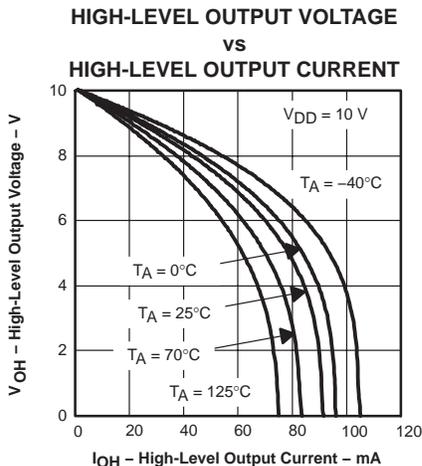
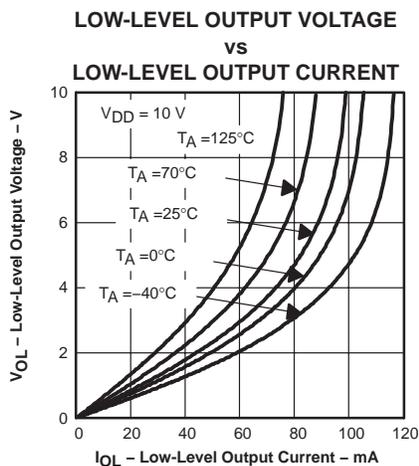
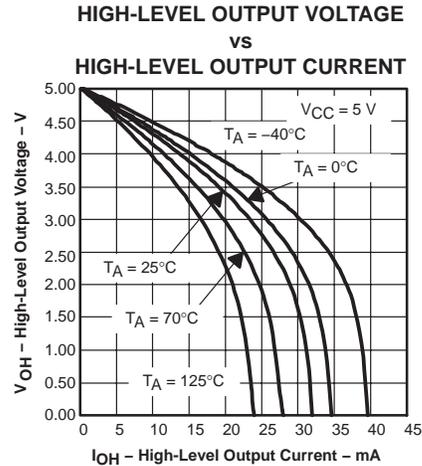
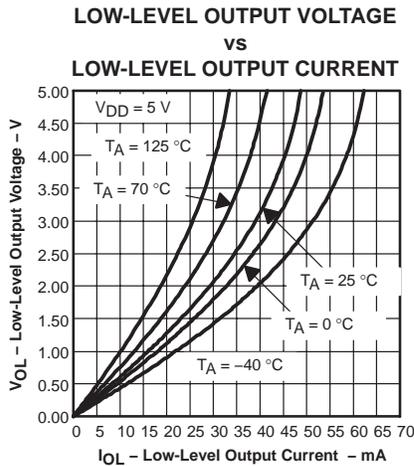
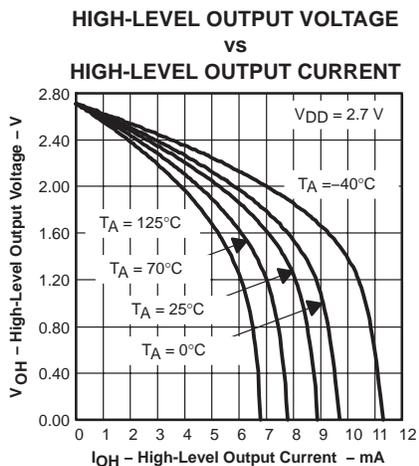
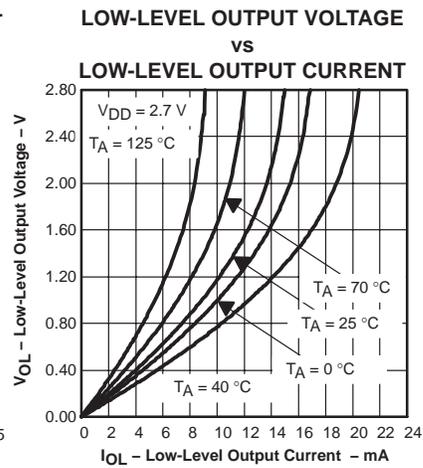
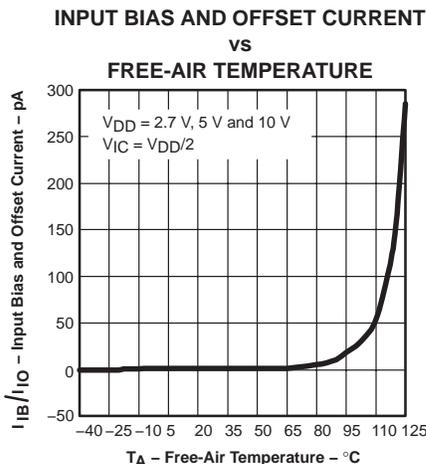
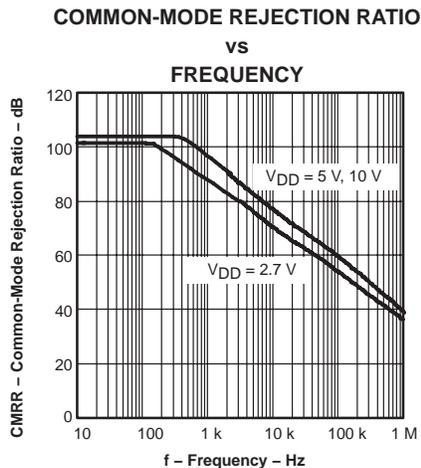
Table of Graphs

| | | | FIGURE |
|--------------------|--|------------------------------|---------------|
| CMRR | Common-mode rejection ratio | vs Frequency | 1 |
| | Input bias and offset current | vs Free-air temperature | 2 |
| V _{OL} | Low-level output voltage | vs Low-level output current | 3, 5, 7 |
| V _{OH} | High-level output voltage | vs High-level output current | 4, 6, 8 |
| V _{O(PP)} | Peak-to-peak output voltage | vs Frequency | 9 |
| I _{DD} | Supply current | vs Supply voltage | 10 |
| PSRR | Power supply rejection ratio | vs Frequency | 11 |
| A _{VD} | Differential voltage gain & phase | vs Frequency | 12 |
| | Gain-bandwidth product | vs Free-air temperature | 13 |
| SR | Slew rate | vs Supply voltage | 14 |
| | | vs Free-air temperature | 15 |
| ϕ_m | Phase margin | vs Capacitive load | 16 |
| V _n | Equivalent input noise voltage | vs Frequency | 17 |
| | Voltage-follower large-signal pulse response | | 18, 19 |
| | Voltage-follower small-signal pulse response | | 20 |
| | Inverting large-signal response | | 21, 22 |
| | Inverting small-signal response | | 23 |
| | Crosstalk | vs Frequency | 24 |

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TYPICAL CHARACTERISTICS



TLV271, TLV272, TLV274

FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS351D – MARCH 2001 – REVISED FEBRUARY 2004

TYPICAL CHARACTERISTICS

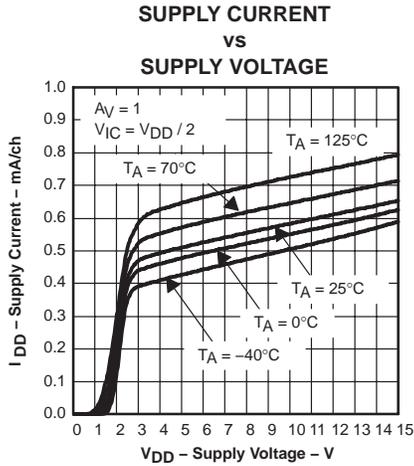


Figure 10

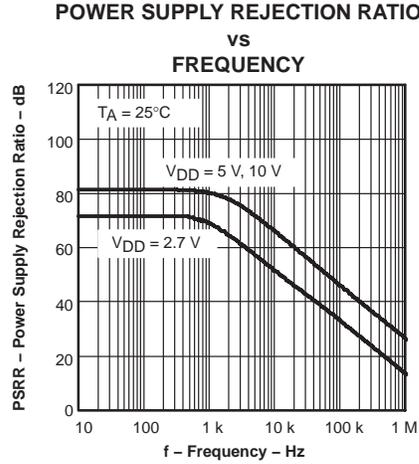


Figure 11

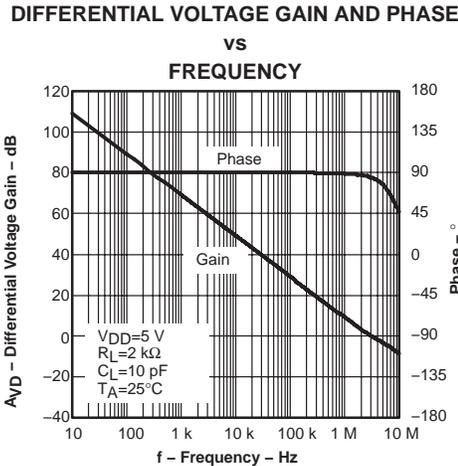


Figure 12

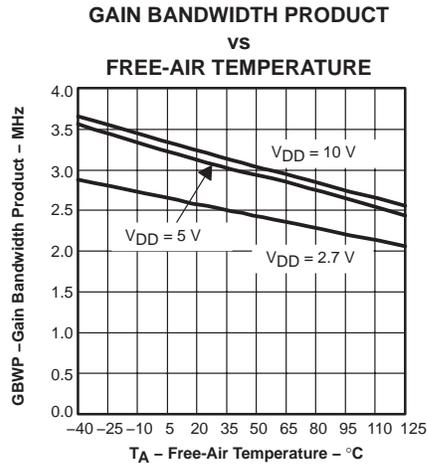


Figure 13

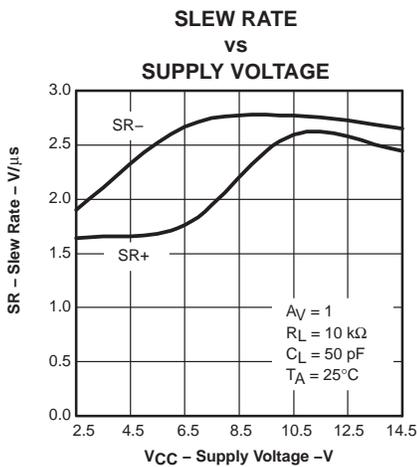


Figure 14

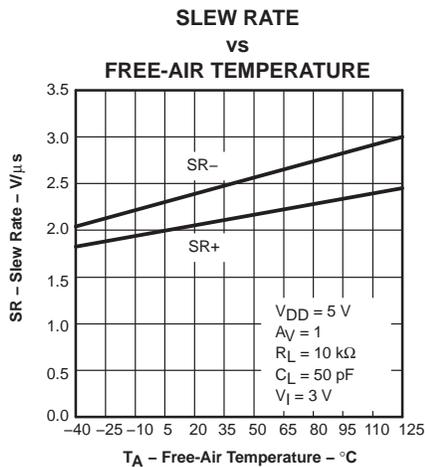


Figure 15

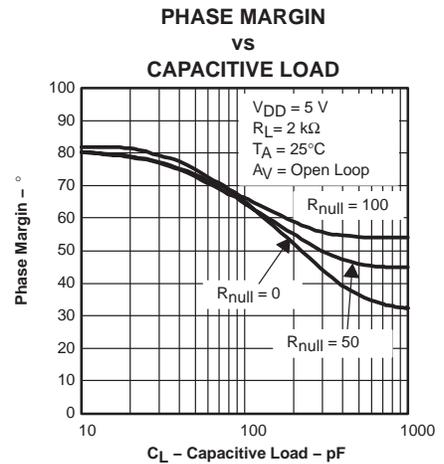


Figure 16

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE

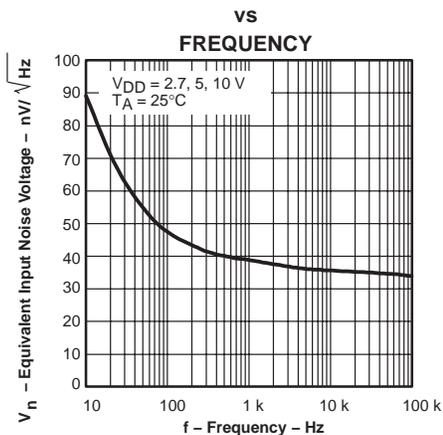


Figure 17

VOLTAGE-FOLLOWER LARGE-SIGNAL
 PULSE RESPONSE

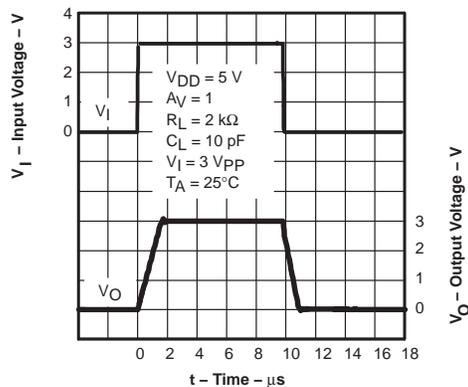


Figure 18

VOLTAGE-FOLLOWER LARGE-SIGNAL
 PULSE RESPONSE

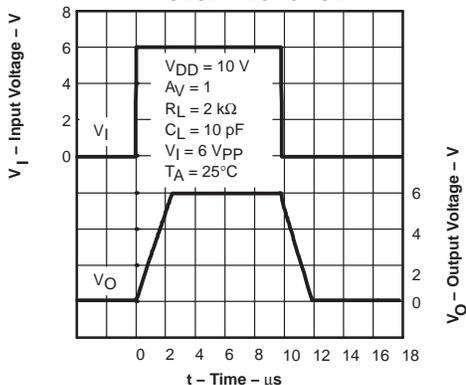


Figure 19

VOLTAGE-FOLLOWER SMALL-SIGNAL
 PULSE RESPONSE

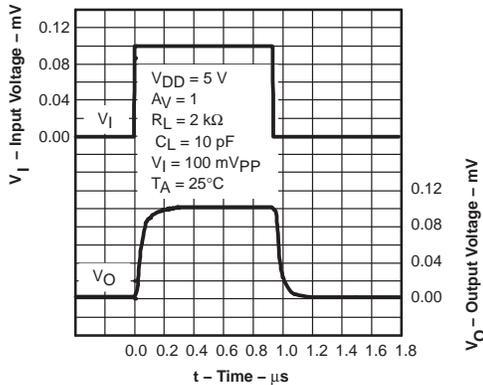


Figure 20

INVERTING LARGE-SIGNAL RESPONSE

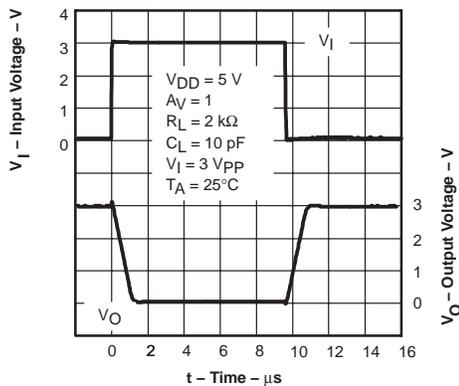


Figure 21

INVERTING LARGE-SIGNAL RESPONSE

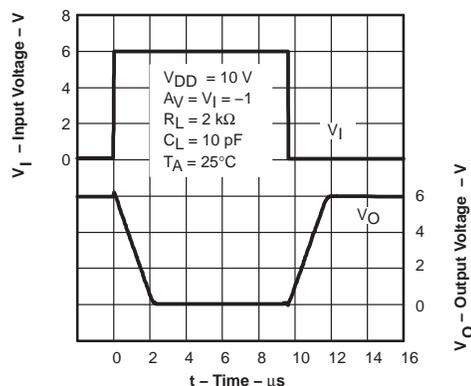


Figure 22

TLV271, TLV272, TLV274

FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL RESPONSE

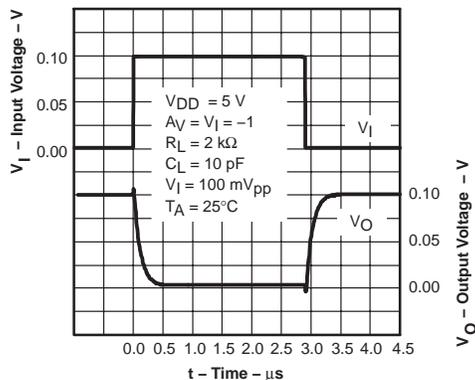


Figure 23

CROSSTALK
VS
FREQUENCY

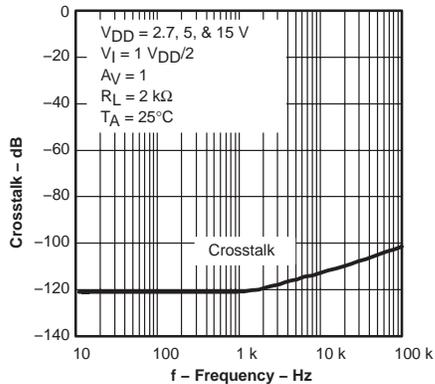


Figure 24

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 25. A minimum value of 20 Ω should work well for most applications.

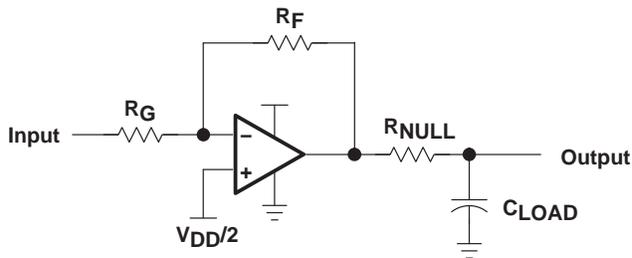


Figure 25. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

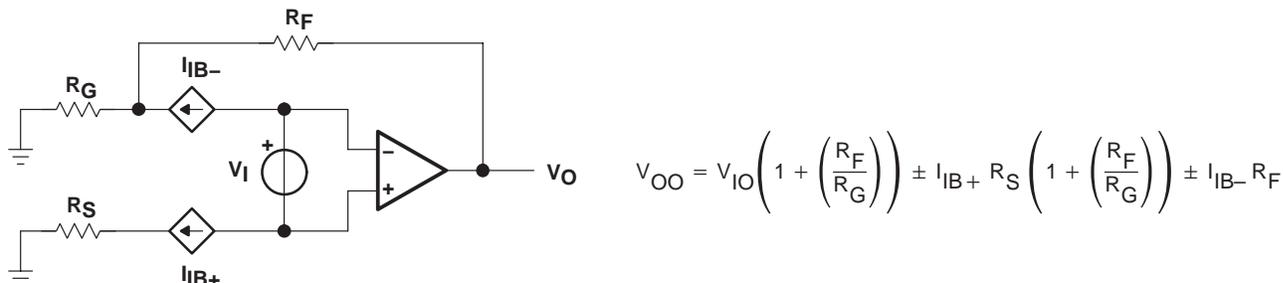


Figure 26. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 27).

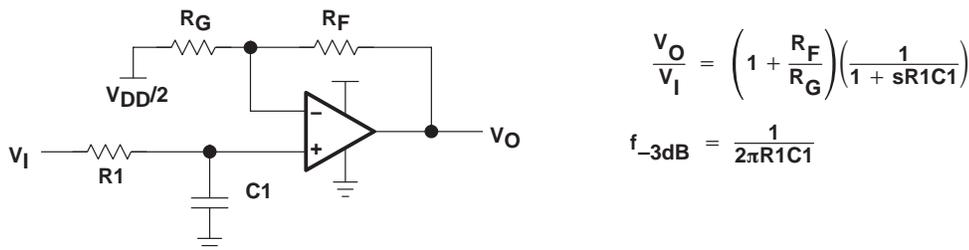


Figure 27. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

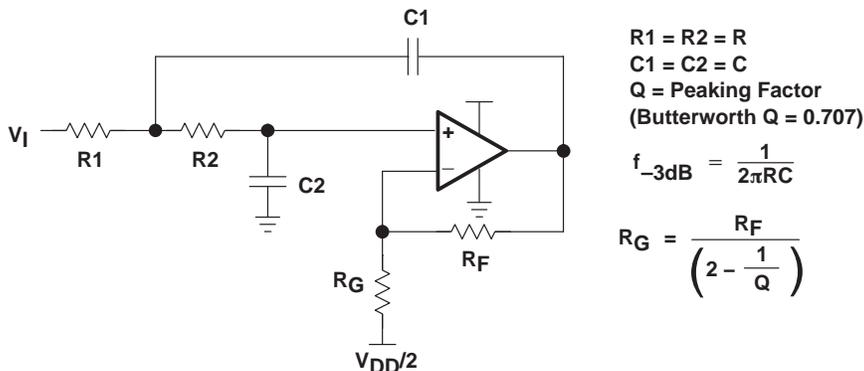


Figure 28. 2-Pole Low-Pass Sallen-Key Filter

TLV271, TLV272, TLV274

FAMILY OF 550- μ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV27x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

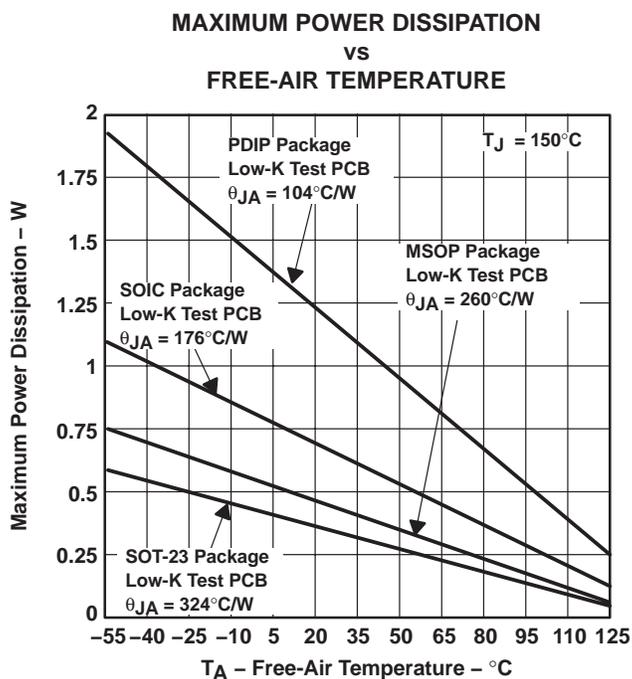
general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 29 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of TLV27x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 29. Maximum Power Dissipation vs Free-Air Temperature

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV271CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T271C | Samples |
| TLV271CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBHC | Samples |
| TLV271CDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBHC | Samples |
| TLV271CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBHC | Samples |
| TLV271CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBHC | Samples |
| TLV271CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T271C | Samples |
| TLV271CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T271C | Samples |
| TLV271CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T271C | Samples |
| TLV271ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T271I | Samples |
| TLV271IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBHI | Samples |
| TLV271IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBHI | Samples |
| TLV271IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBHI | Samples |
| TLV271IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBHI | Samples |
| TLV271IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T271I | Samples |
| TLV271IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | T271I | Samples |
| TLV271IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | T271I | Samples |
| TLV272CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T272C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|----------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV272CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T272C | Samples |
| TLV272CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AVF | Samples |
| TLV272CDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AVF | Samples |
| TLV272CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | AVF | Samples |
| TLV272CDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AVF | Samples |
| TLV272CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T272C | Samples |
| TLV272CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T272C | Samples |
| TLV272ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | Samples |
| TLV272IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | Samples |
| TLV272IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AVG | Samples |
| TLV272IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AVG | Samples |
| TLV272IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AVG | Samples |
| TLV272IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AVG | Samples |
| TLV272IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | Samples |
| TLV272IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T272I | Samples |
| TLV272IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | T272I | Samples |
| TLV272IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | T272I | Samples |
| TLV274CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV274CDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274CPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV274C | Samples |
| TLV274ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV274I | Samples |
| TLV274INE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV274I | Samples |
| TLV274IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |
| TLV274IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV274I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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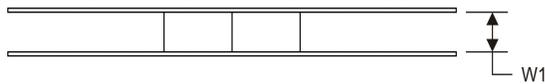
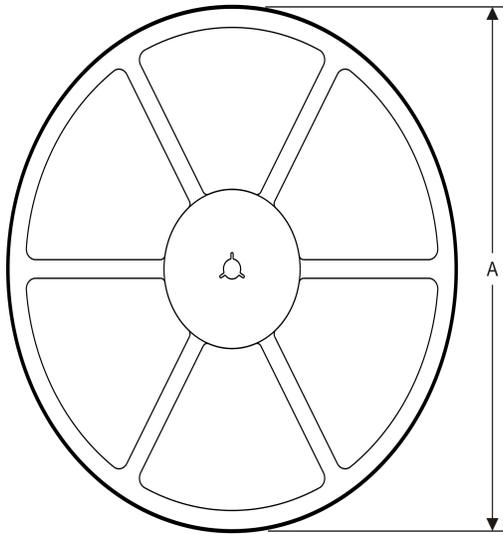
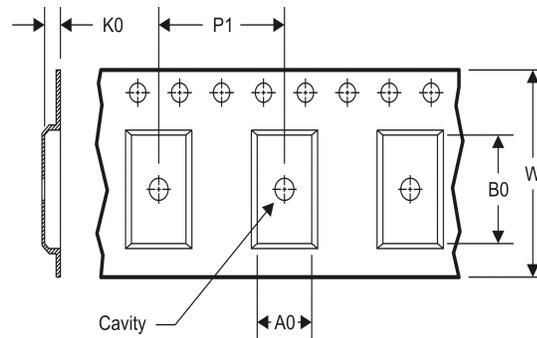
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OTHER QUALIFIED VERSIONS OF TLV271, TLV272, TLV274 :

- Automotive: [TLV271-Q1](#), [TLV272-Q1](#), [TLV274-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

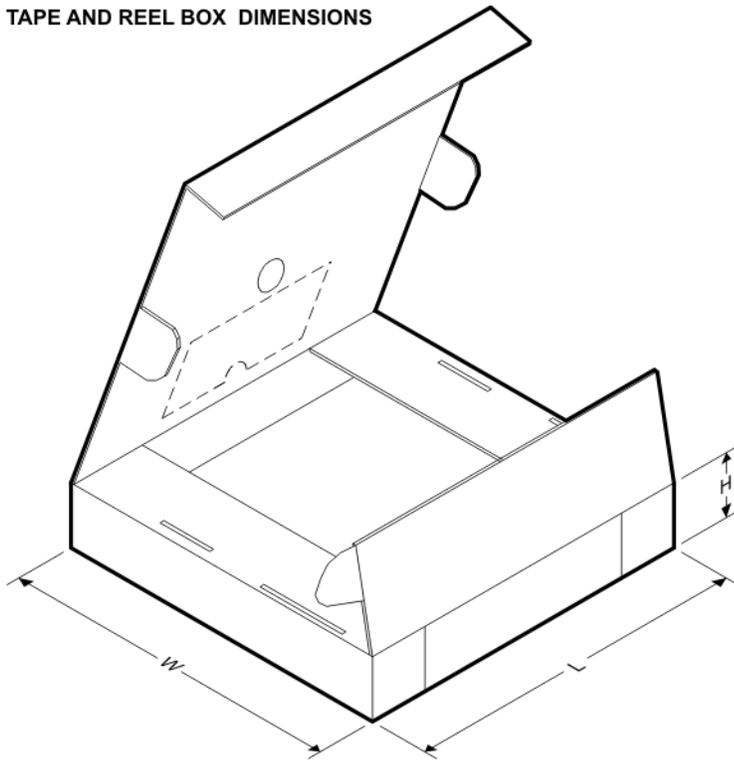
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV271CDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV271CDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV271CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV271IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV271IDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV272IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV274CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV274CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV274IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV274IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

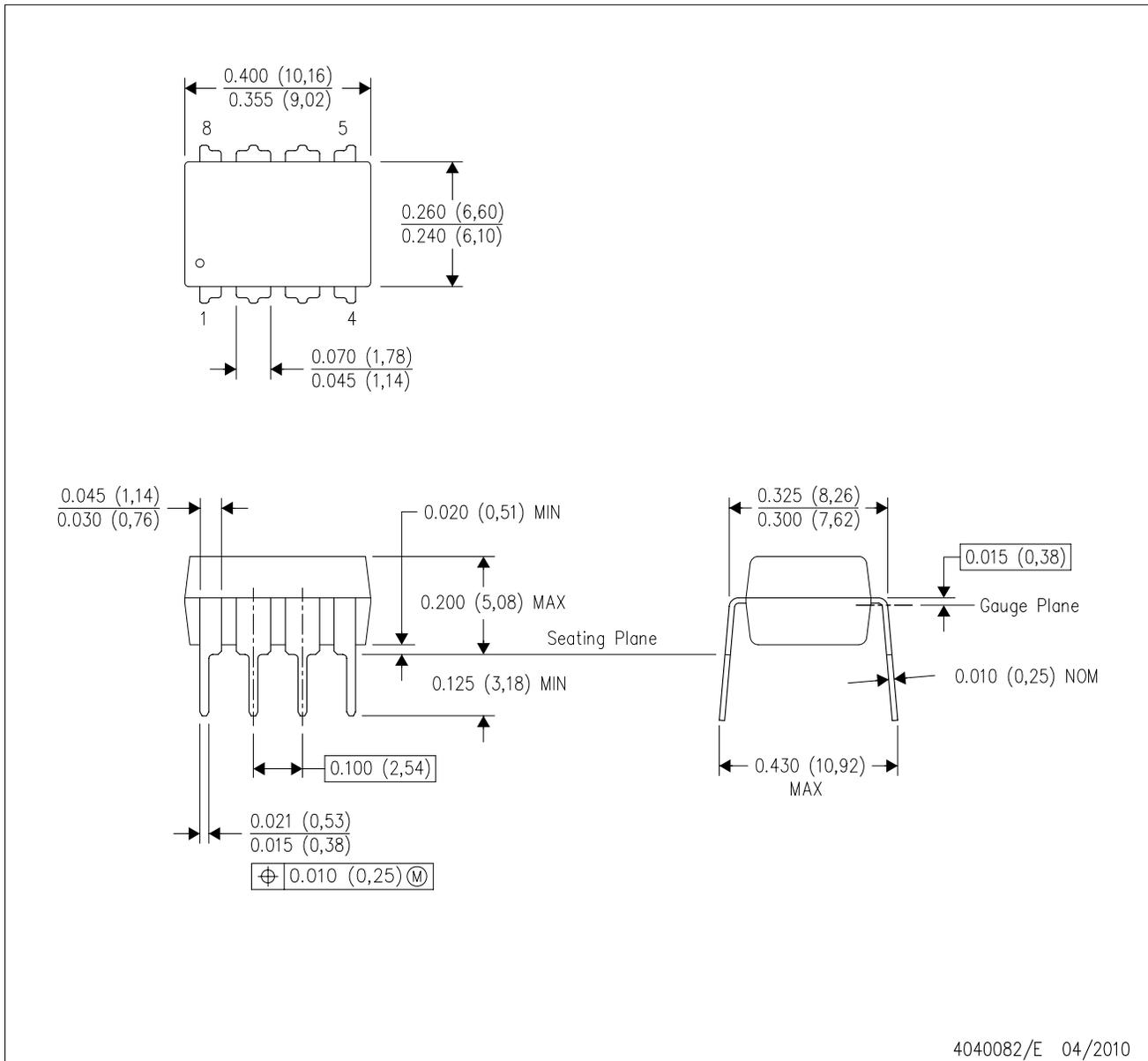
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV271CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV271CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV271CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV271IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV271IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV272CDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV272CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV272IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV272IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV274CDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV274CPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV274IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV274IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

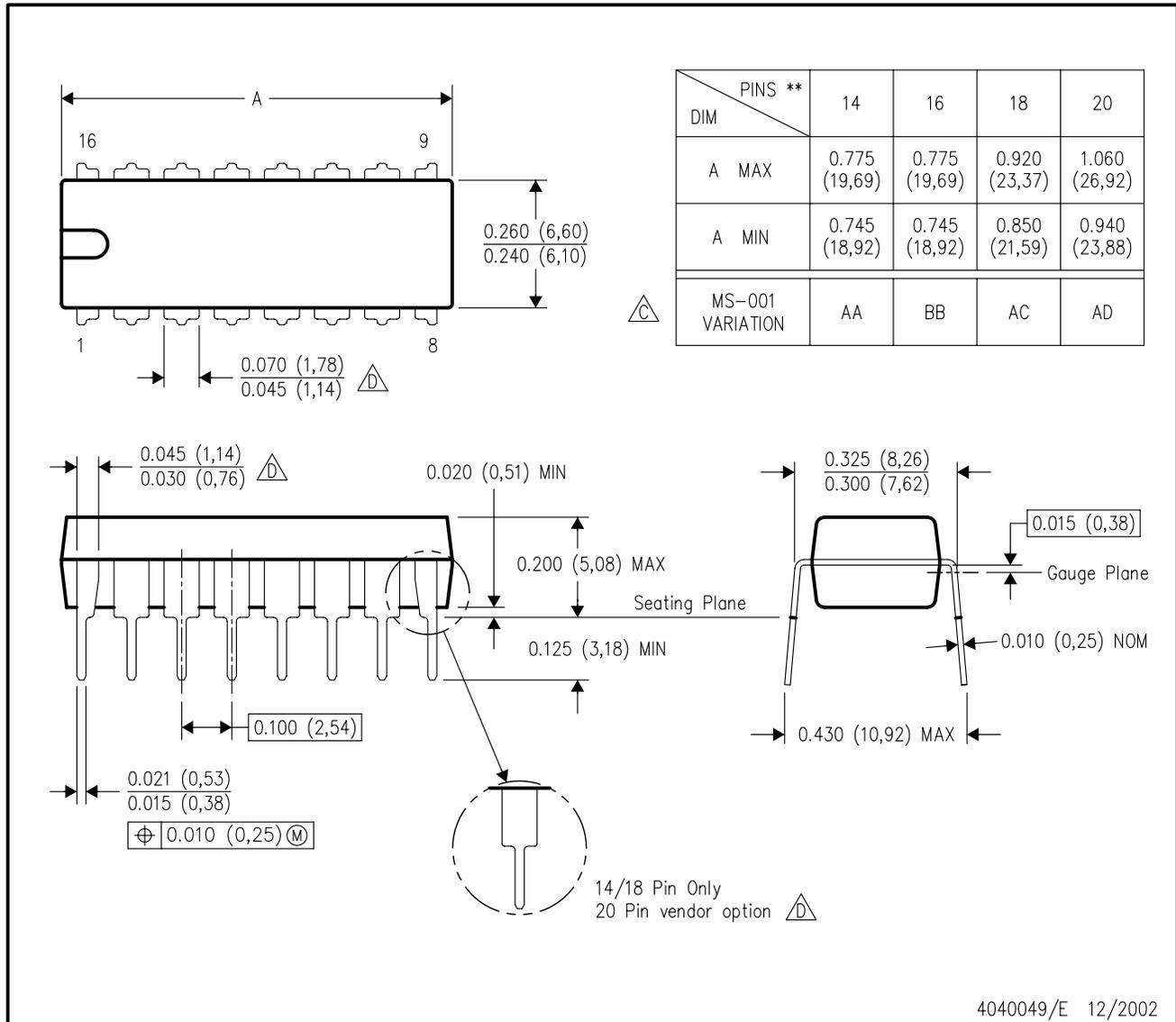


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

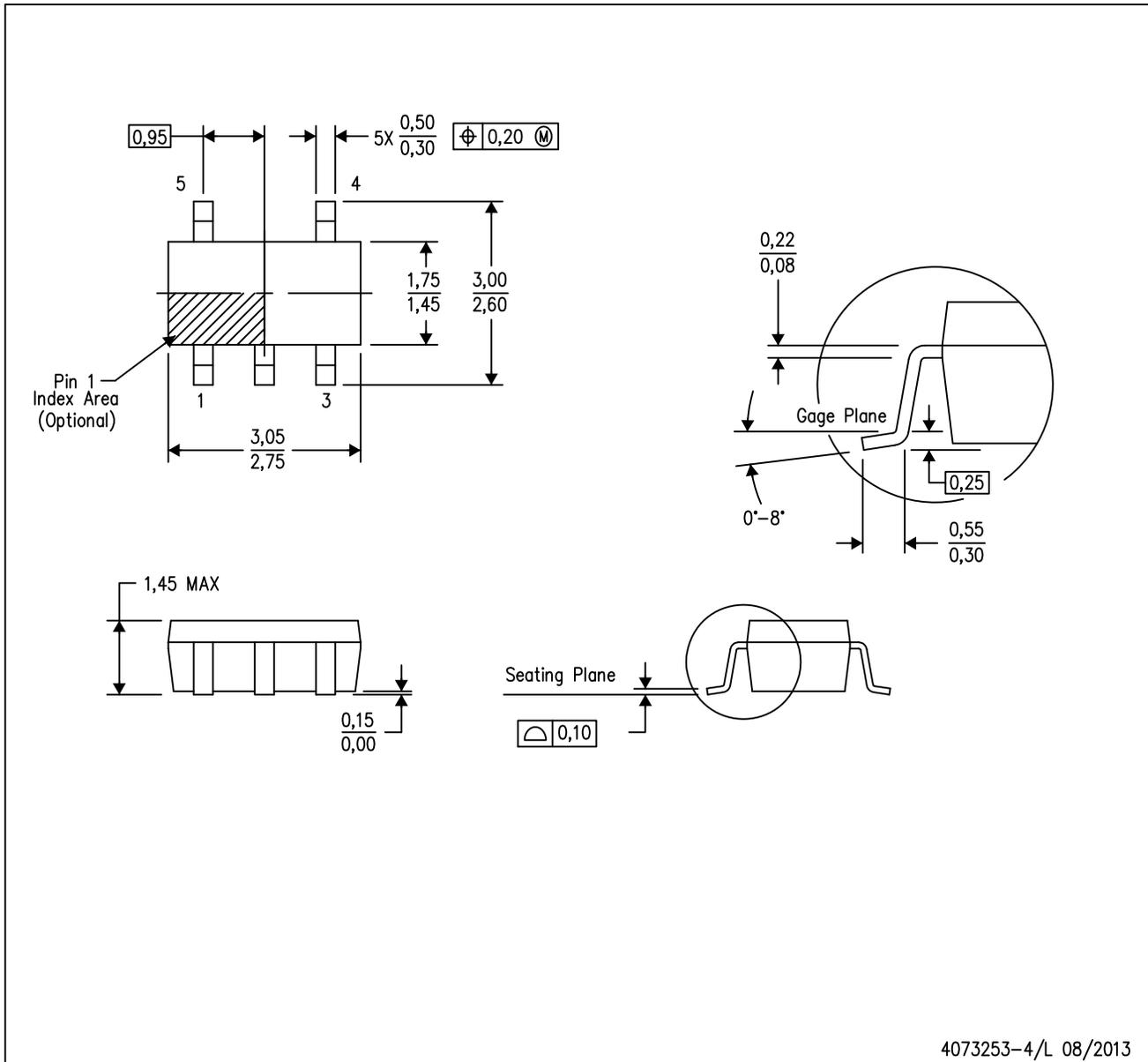
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DBV (R-PDSO-G5)

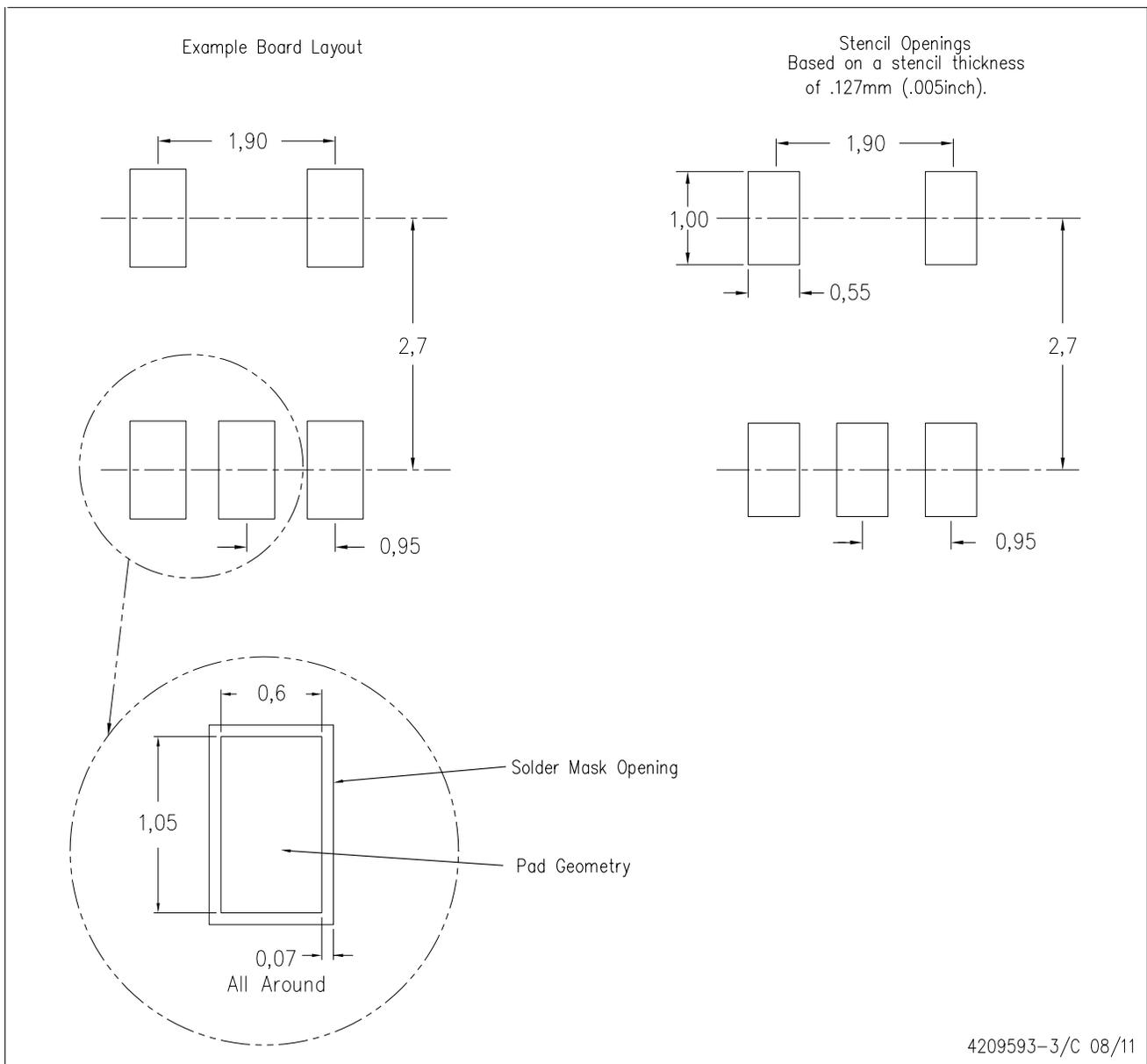
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

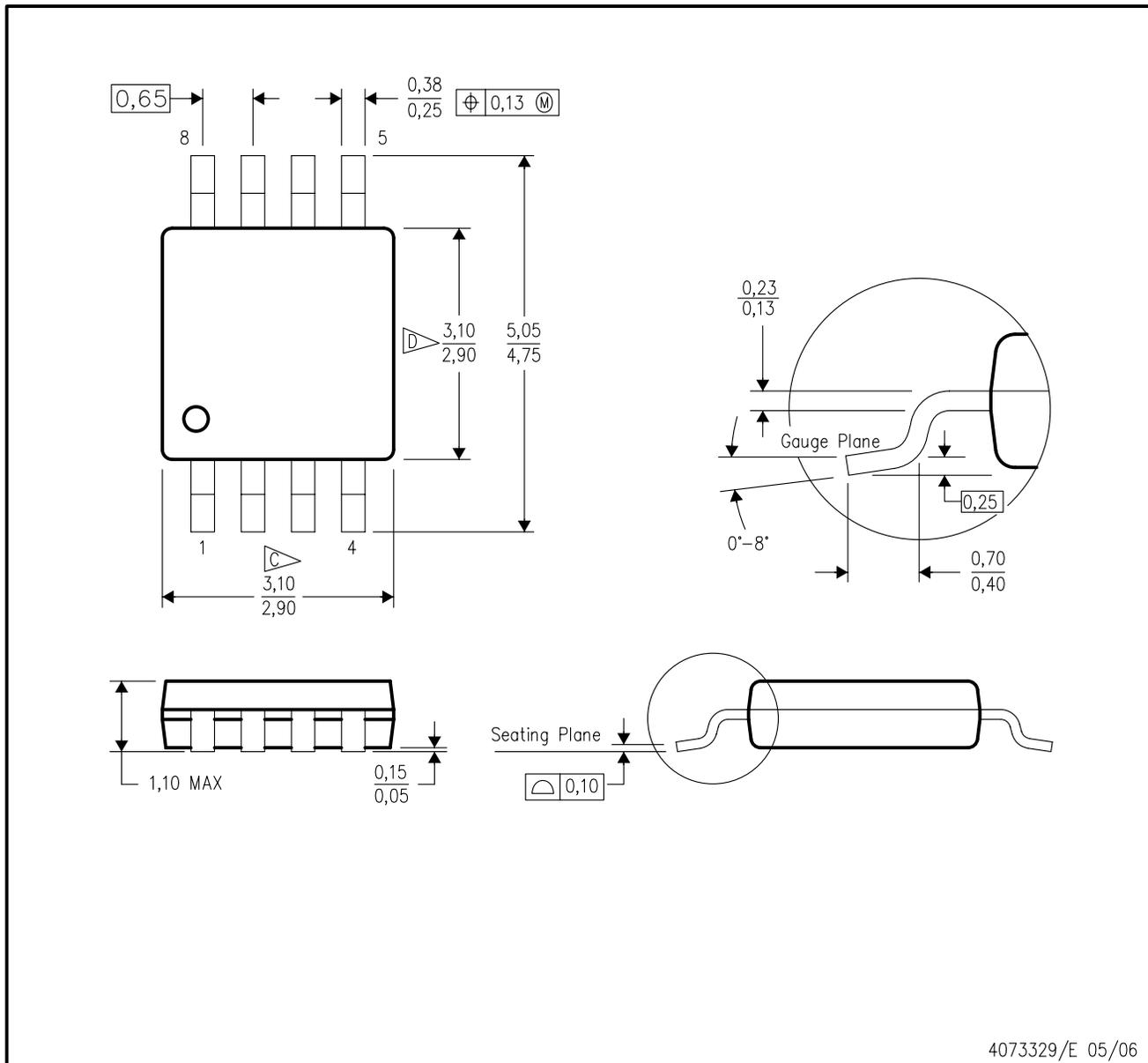
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

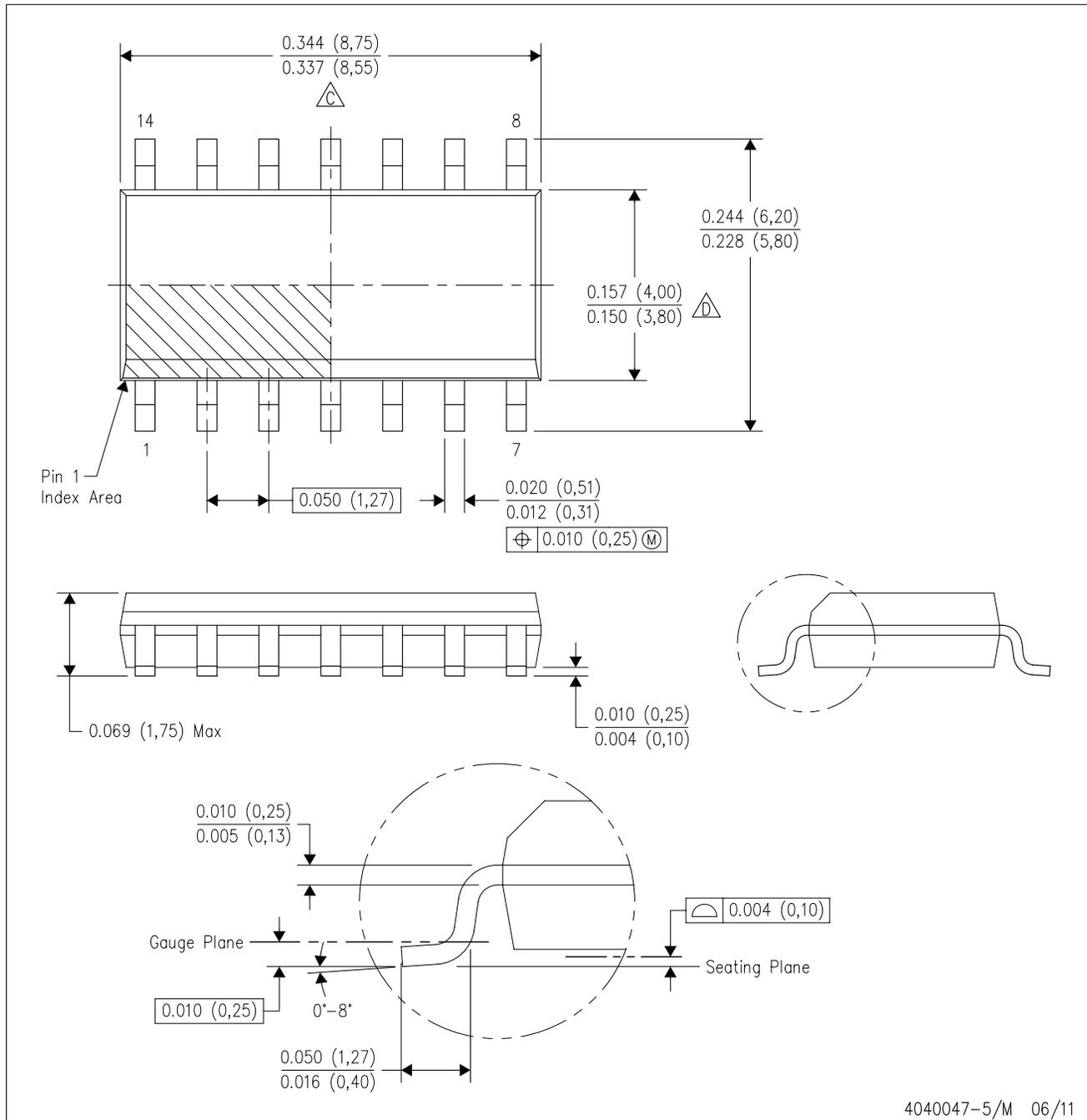
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G14)

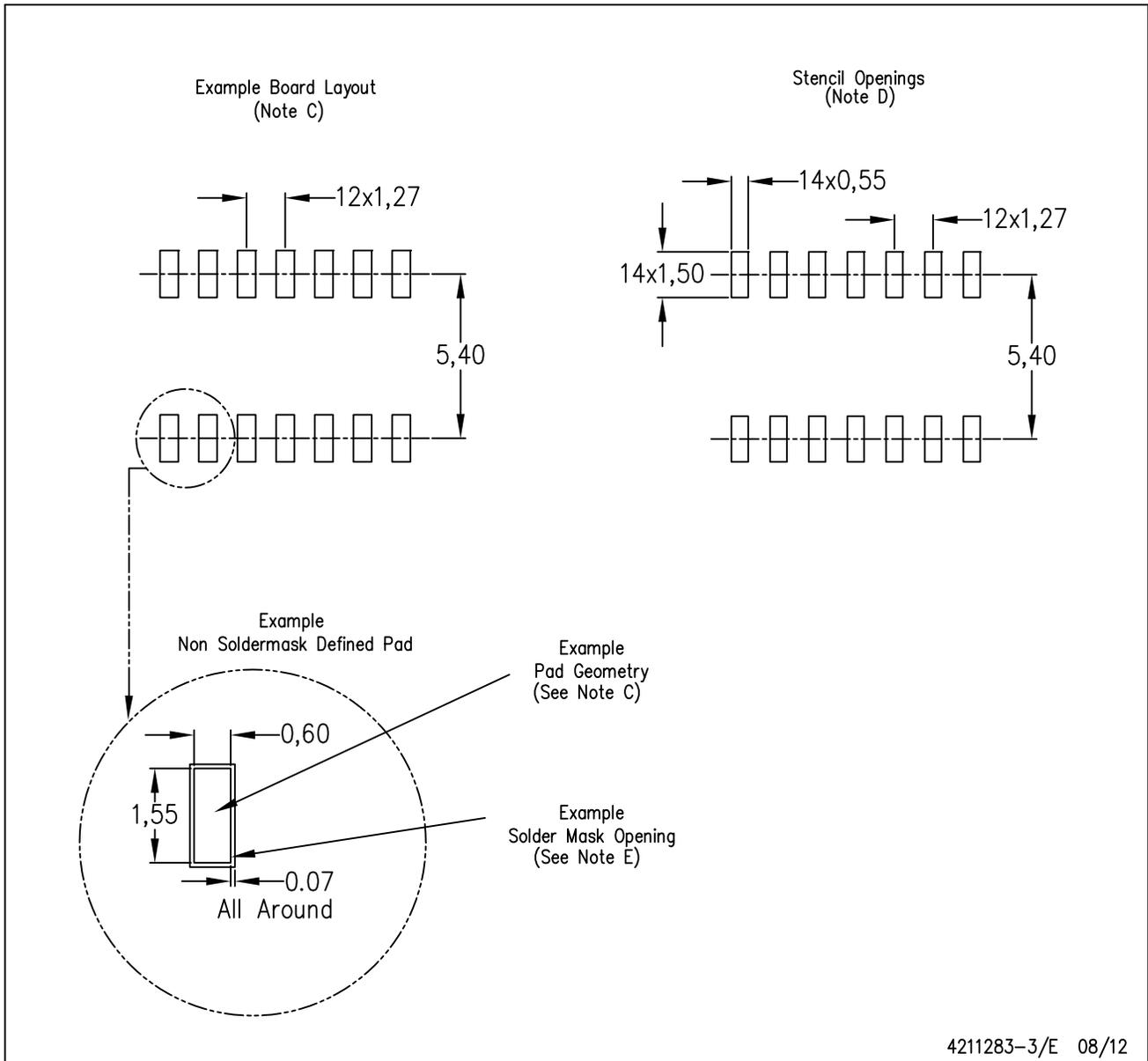
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

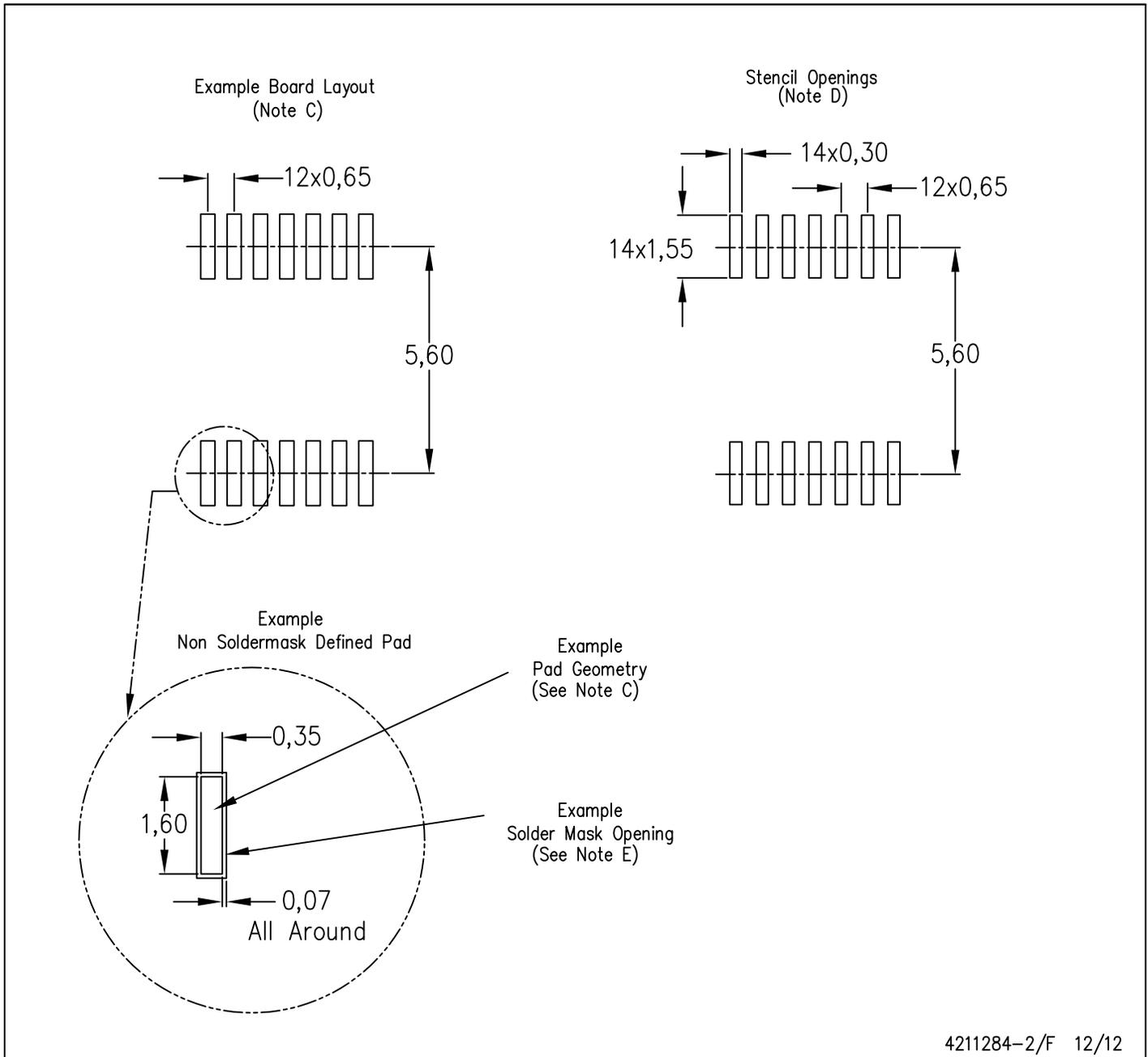


4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

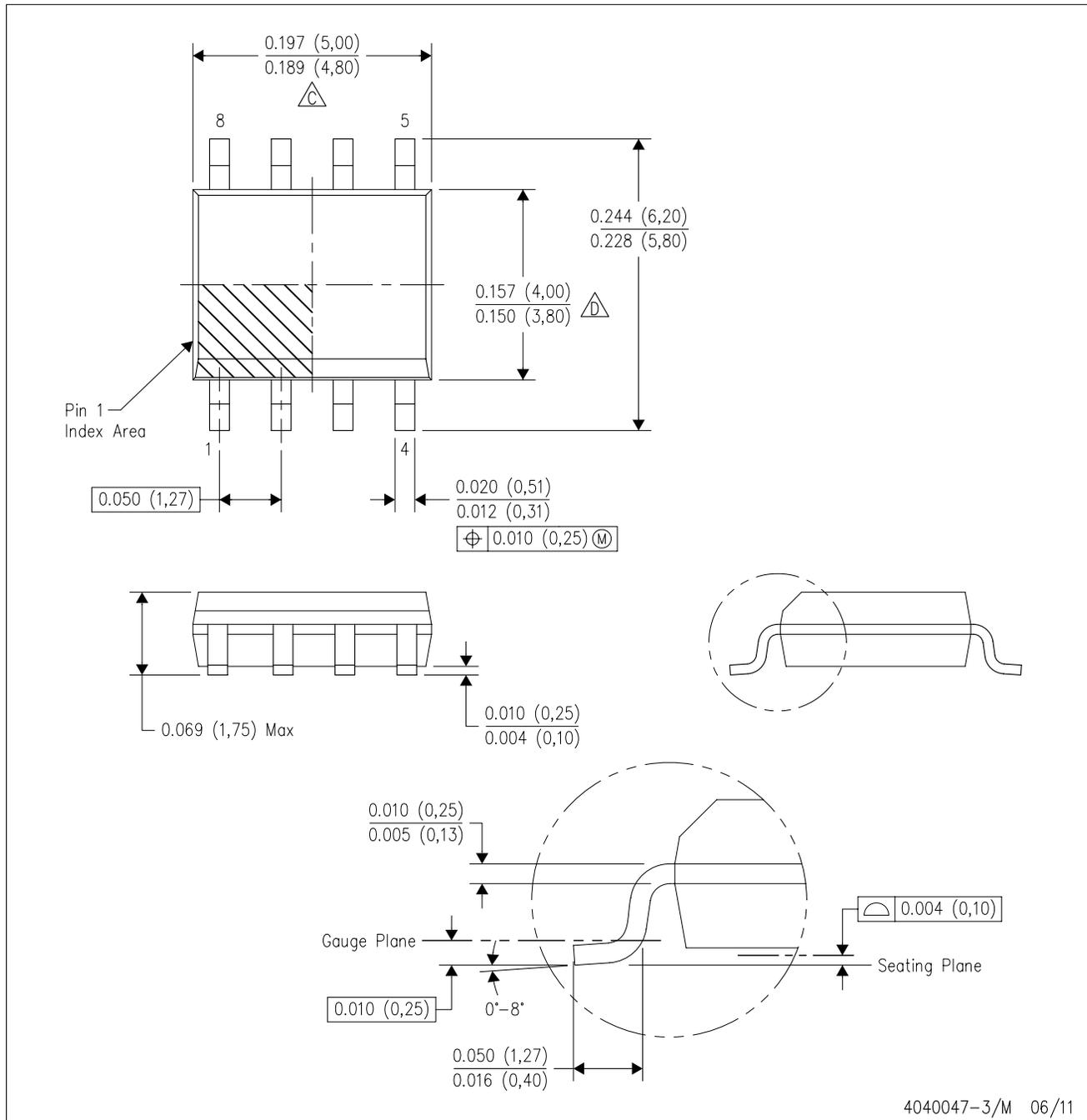
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

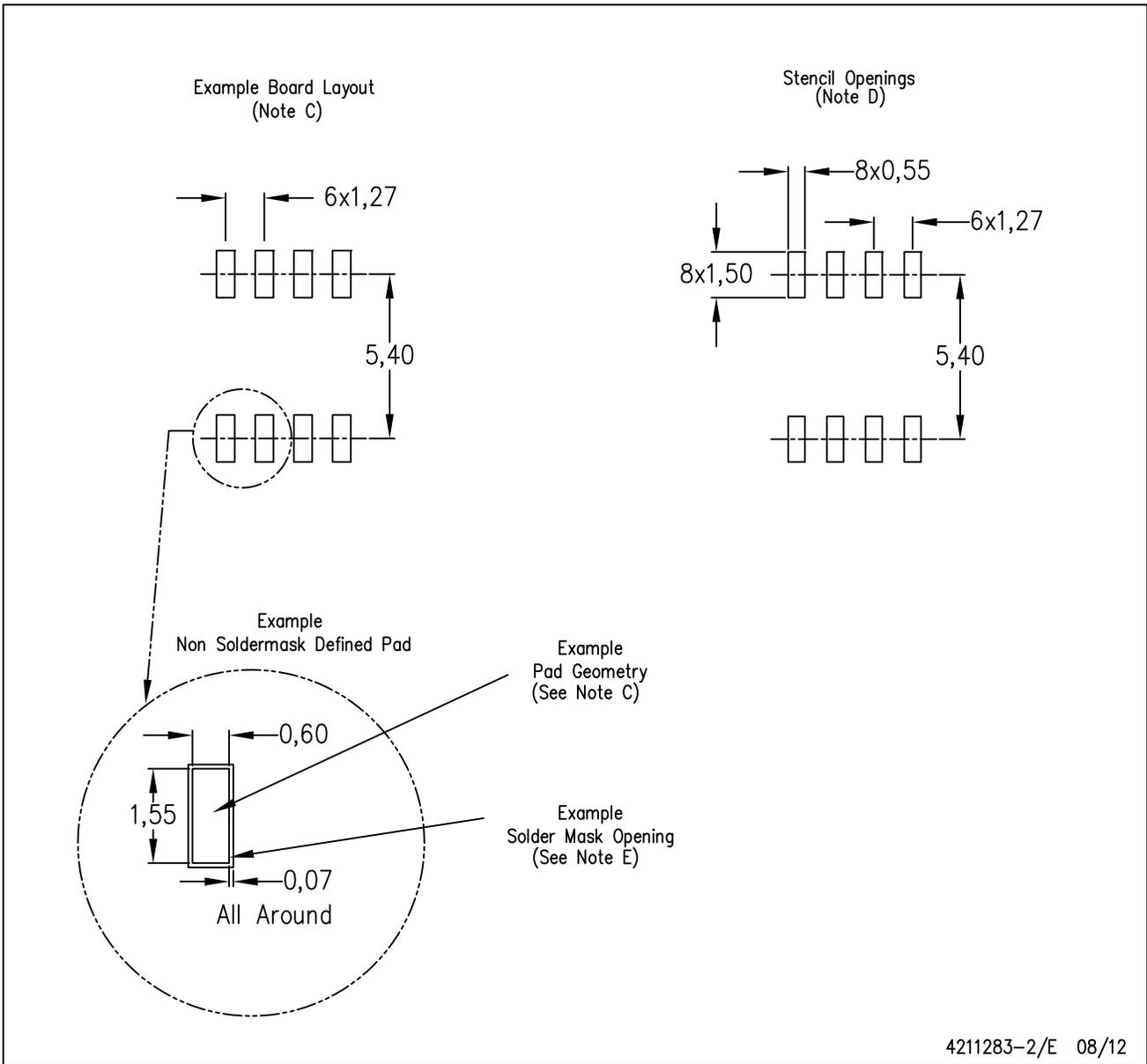
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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